Q.P. Code: 20EC4205 **R20**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

M.Tech I Year I Semester Regular Examinations July-2021

VERILOG HDL

(VLSI)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Explain structure design methodology with the verilog HDL.	L2	**6M**
	b	Explain hardware modeling verilog primitives.	L2	**6M**
		OR		
2	**a**	Write verilog HDL structural model for a full sub tractor using NAND gates	L3	**6M**
	b	Illustrate behavioral description in verilog.	L3	**6M**
		UNIT-II		
3	**a**	What is user defined primitives? Explain combinational behavior of user defined primitives.	L1	**7M**
	b	Explain conditional operator, operator precedence in VERILOG.	L2	**5M**
		OR		
4		Explain in detail about verilog HDL data types with suitable examples.	L2	**12M**
		UNIT-III		
5	**a**	Explain behavioral statements in verilog HDL.	L1	**6M**
	b	Write a short note on intra assignment delay.	L2	**6M**
		OR		
6	**a**	Write short notes on non-blocking assignments and what are the sequences takes place at each positive edge of clock for the non-blocking assignments.	L3	**7M**
	b	Explain behavioral models of finite state machine.	L1	**5M**
		UNIT-IV		
7	**a**	Draw the block diagram for HDL based synthesis explain each block	L1	**6M**
	b	Draw the block diagram for test bench for post synthesis design verifications.	L4	**6M**
		OR		
8	**a**	Explain the tree state buffers.	L3	**6M**
	b	Discuss about behavioral synthesis.	L2	**6M**
		UNIT-V		
9	**a**	Discuss why switch level is useful.	L3	**7M**
	b	Give the MOS transistor technology.	L1	**5M**
		OR		
10	**a**	Write and verify a switch level al a three input static CMOS NOR gate.	L3	**6M**
	b	Explain the truth table for switch level MOSFET transistor module.	L2	**6M**

*** END ***